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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/684,160	10/04/2000	James Daniel Merchant	CYPR-CD00055.US.P	1666

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EXAMINER	
HAMILTON, MONPLAISIR G	

ART UNIT	PAPER NUMBER
2135	16

DATE MAILED: 07/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/684,160	Applicant(s) MERCHANT ET AL.
	Examiner Monplaisir G Hamilton	Art Unit 2135

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13 and 21-25* is/are pending in the application.

4a) Of the above claim(s) *12 and 14-20* is/are withdrawn from consideration.

5)☐ Claim(s) *22-25* is/are allowed.

6)☒ Claim(s) *1-4 and 8* is/are rejected.

7)☒ Claim(s) *5-7 and 9-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/22/04 has been entered.

Claims 1-21 were pending. The communication filed on 3/22/04 amended Claims 1-3, 5-6, 8-11, 13 and 21, cancelled Claims 12 and 14-20 and added Claims 22-25. Claims 1-11, 13 and 21-25 remain for examination.

Response to Arguments

2. Applicant's arguments, see Paper No. 15, filed 3/22/04, with respect to the rejection(s)of Claims 1-13 and 21under 103(a) as being unpatentable over Mason et al. (US 5,946,219) in view of Varadarajan (US 5,838,583) and Claims 14-21 under 103(a) as being unpatentable over Mason et al. (US 5,946,219), have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-4 are rejected under the judicially created doctrine of double patenting over Claims 1-3 and 10 of U. S. Patent No. US 6,490,712 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

Double Patenting	
Application 09684160, Claims 1-4	US 6,490,712 Claims 1-3 and 10
1. A computer implemented method of generating an order of loading data into a programmable device comprising the steps of: a) automatically identifying a plurality of configuration bits for programming a programmable device by traversing a hierarchical schematic representation of the programmable device;	1. A computer implemented method of determining addresses of configuration cells in a schematic hierarchy of a circuit design comprising the steps of: a) accessing said schematic hierarchy of said circuit design; b) automatically traversing said schematic hierarchy to identify a configuration cell;

b) automatically determining a plurality of addresses corresponding to said **plurality of configuration bits, said plurality of addresses being in an address space of a memory of the programmable device and operable to store configuration bits for programming the programmable device**;	c) automatically determining an address for said *configuration cell*;
c) automatically determining a plurality of logical names for said plurality of configuration bits; and	d) automatically determining a unique name for said configuration cell including a hierarchical logical name and a schematic path name;
d) based on an order in which said address space is traversed plurality when programming said programmable device, automatically storing said plurality of logical names for said plurality of configuration bits within a data structure within computer readable memory, wherein said data structure **describes an order** in which to program said programmable device.	e) automatically associating and storing said name and said address of said configuration cell within a data structure within computer readable memory; and f) repeating said steps b)-e) for each configuration cell of said schematic hierarchy.
2. The method of Claim 1 wherein step a) comprises the step of:	2. The method of claim 1 wherein step c) comprises the steps of:
a1) identifying configuration bits of said plurality of configuration bits, which are at the lowest level in said hierarchical schematic representation.	c1) automatically determining a wordline associated with said configuration cell; and c2) automatically determining a bitline associated with said configuration cell. 3. The method of claim 1 wherein step b) comprises the step of:

3. The method of Claim 1 wherein step b) comprises the steps of:	b1) automatically traversing said schematic hierarchy to identify a configuration cell which is at the lowest level in said schematic hierarchy.
b1) determining a wordline associated with a configuration bit of said plurality of configuration bits; and b2) determining a bitline associated with said configuration bit of said plurality of configuration bits.	10. The method of claim 1 wherein said schematic hierarchy is of a complex programmable logic device (CPLD).
4. The method of Claim 1 further comprising the step of:	
e) repeating said steps a) through d) for each configuration block of said programmable device.	

Claims 1-4 of the current application differ from Claims 1-3 and 10 of US 6,490,712 in the use of the claimed data structure. Claims 1-4 of the current application cites the data structure as using information for configuration bits whereas US 6,490,712 cites the data structure as storing information corresponding to configuration cells. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the

teachings of US 6,490,712 such that the data structure stores information about configuration bits. One of ordinary skill in the art would have been motivated to do this because it would allow the system to automatically identify the address of the configuration bits (US 6,490,712: col 2, lines 5-30).

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Varadarajan et al (US 5,838,583).

Referring to Claim 8:

Varadarajan discloses a computer implemented method of generating an order of loading data into a programmable logic device comprising the steps of:

a) accessing a data structure comprising a plurality of logical names corresponding to a plurality of addresses in an address space of a memory operable to store configuration bits for programming a programmable logic device (col 8, lines 5-65);

b) accessing a data structure specifying an order in which said plurality of addresses are traversed when loading said configuration bits into said programmable logic device (col 8, line 60-col 9, line10);

c) automatically ordering said plurality of logical names from step a) based on the order specified in said data structure in step b) and information in the data structure comprising the plurality of logical names corresponding to the plurality of addresses (col 9, lines 25-65);

and

d) automatically storing said ordered plurality of logical names from step c) in a

data structure within computer readable memory, wherein said ordered plurality of logical names describe an order of loading said configuration bits into said programmable logic device (col 10, lines 1-25).

Allowable Subject Matter

5. Claims 22-25 are allowed.

Claims 5-7 and 9-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monplaisir G Hamilton whose telephone number is (703) 305-5116. The examiner can normally be reached on Monday - Friday (8:00 am - 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y Vu can be reached on (703) 305-4393. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AU 2135

Monplaisir Hamilton